Claim rejections - 35 U.S.C. § 103(a)

1. Reconsideration of the rejection of claims 13-16 and 18-24 under 35 U.S.C 103(a) as being unpatentable over Yamai (JP 409045691) in combination with Forehand et al. (U.S. Patent 5,847,936) and Mars (U.S. Patent 5,795,81) is respectfully requested based on the following.

In review, the instant invention provides for semiconductor devices having fine-pitch solder bumps over the surface thereof.

By applying fine pitch solder bumps directly to the I/O pads of a semiconductor device, the instant invention:

- enables that a redistribution interface is no longer needed, allowing for bonding the semiconductor device directly to a Ball Grid Array substrate using the flip-chip bonding approach
- provides for shortening the interconnection between a semiconductor device and the substrate on which the device is mounted, thus improving the electrical performance of the device
- further provides for the elimination of conventional methods of re-distribution of device I/O interconnect, making

packaging of the device more cost-effective and eliminating performance degradation

- further provides for improved chip accessibility during testing of the device, thus eliminating the need for special test fixtures
- further provides for improvements in performance and device reliability of BGA packages that are used for the mounting of semiconductor devices having small-pitch I/O interconnect bumps, and
- further provides for a method of mounting small-pitch semiconductor devices in such a manner that flux removal and the dispensing of device encapsulants is improved.

The fine-pitch, high reliability solder bumps of the instant invention are specified in detail in dependent claim 18 of the instant invention.

Yamai (JP 409045691) does not provide for an array of fine pitch solder bumps. Yamai provides for a "large-diameter" pillar shaped part **and** a "small-diameter pillar-shaped part". However the final pillar shaped interconnects that are provided by Yamai, Fig. 6b, have no correspondence or similarity with the cross section or the composition of the solder bumps of the

instant invention as shown in Figs. 3 and 4 of the instant invention.

The solder bump that is provided by Yamai comprises several distinct elements, Fig. 1 of Yamai, as follows:

1. a contact pad 2 is provided over a semiconductor surface 1, the contact pad is exposed through and surrounded by patterned passivation layer 3
2. a patterned carene film 4 and a patterned diffusion preventing film 5 are provided aligned with the contact pad 2, these films are removed where they do not align with the contact pad 2; the carene film serves as an electrode for subsequent electroplating
3. a first bump 10 is formed over the diffusion preventing film 5, comprising a lower part 10b being a cylindrical large-diameter pillar shaped part over the diffusion preventing film 5 and a upper small diameter pillar shaped part 10a over the lower part 10b, both parts being formed of the same solder material having a high melting point, and
4. a second bump 11, having the same diameter as the large-diameter part 10b, over the first bump 10, formed of a solder material having a melting point that is lower than the first bump 10.

The instant invention is based as an application of the solder balls that are shown in cross section in Figs. 3 and 4 of the instant invention.

These solder bumps, as stated on page 13 of the specification of the instant invention, provide:

- a fine-pitch solder bump
- smaller solder bumps
- a fine-pitch solder bump of high reliability due to the increased height of the solder bump
- a cost-effective solder bump by using standard solder material and eliminating the need for expensive "low-α solder"
- a solder bump that allows easy cleaning of flux after the process of flip chip assembly and before the process of underfill and encapsulation, and
- a solder bump which allows easy application of underfill.

The structure of the solder bump that is provided by Yamai, does not provide for the structure that is provided by the instant invention of the solder bump that, see claim 18 of the instant invention:

- is created over a semiconductor surface such as the surface of a substrate
- comprises a layer of dielectric that has been deposited over the semiconductor surface
- comprises contact pads that have been created on the surface of a layer of dielectric
- comprises a patterned layer of passivation deposited over the surface of the layer of dielectric
- comprises an isotropically etched layer of barrier metal, completely removing the barrier metal from the surface of the layer of passivation except where the barrier metal is covered by the overlying pillar metal of the solder bump, and
- comprises a layer of under bump metal created overlying the pillar metal of the solder bump

By anisotropically etching the layer of barrier metal, Fig. 4 of the instant invention, the barrier layer protrudes from the pillar metal of the solder bump.

The cross section shown by Yamai does not show a complete semiconductor package with for instance, Fig. 5 of the instant invention, contact balls 58, underfill 62 (Fig. 6), molding

compound 60 into which the device 50 is embedded for protection against the environment.

Yamai does not show a solder mask for the reasons as cited above, that is Yamai does not show a semiconductor flip chip device package but merely provides a solder bump for a chip component and its manufacture. Yamai therefore does not provide for creating a semiconductor package whereby small pitch solder bumps are provided over a semiconductor device and whereby the package is created making optimum use of the small pitch solder bumps of the device.

Yamai does also not provide for, as specified in claim 13 of the instant invention:

- a Ball Grid Array substrate having been provided with points of electrical contact over a first and a second surface thereof, the points of electrical contact provided over the second surface of the BGA substrate being connected to interconnect lines provided over the second surface of the BGA substrate
- a solder mask provided over the second surface of the BGA substrate

- a device being positioned over the second surface of the BGA substrate, fine pitch, high reliability solder bumps facing the second surface of the BGA substrate, providing contact between the fine pitch, high reliability solder bumps and the points of electrical contact provided over the second surface of the BGA substrate
- electrical contact having been established between the fine pitch, high reliability solder bumps and the points of electrical contact provided over the second surface of the BGA substrate by a process of solder reflow
- the semiconductor device being encapsulated in a molding compound, the molding compound surrounding the device on all sides including the active surface of the device, and
- the contact balls making electrical contact with the points of electrical contact provided over the first surface of the contact having been established between the solder balls inserted into the solder mask provided over the first surface of the BGA substrate and the points of electrical contact provided over the first surface of the BGA substrate by a process of solder reflow.

Significantly, the difference between Yamai and the instant invention becomes even more pronounced in the supporting claims

of the instant invention, which further highlight the advantages gained with the package of the instant invention, a package that uses fine-pitched solder bumps, which enables:

- claim 14, the solder mask provided over the second surface of said BGA substrate being removed from points of electrical contact provided over the second surface of the BGA substrate by a measurable amount, creating a channel through which cleaning solution can readily flow
- claim 15, the points of electrical contact provided in an active surface of the semiconductor device comprising a peripheral pad design.
- claim 16, the points of electrical contact provided in an active surface of the device comprising a center type pad design
- claim 17, dummy solder bumps having been provided over the active surface of the device, providing mechanical support for the device, the dummy solder bumps being provided in addition to the fine pitch, high reliability solder bumps provided to the points of electrical contact in the active surface of the device.

Mars provides for an interconnection between and Integrated Circuit chip and a supporting substrate. As part of the interconnection provided by Mars, Fig. 6 as referred to by Examiner and related text Col. 8, lines 43 e.a., an isolation layer 601 is patterned such that isolation layer 601 leaves uncovered a portion of the substrate bonding contact 501C. Isolation layer 601 ensures that metallization 502 is applied only to substrate bonding contacts 501C. In other words: the by Examiner referred to "solder mask" as provided by Mars is not really a solder mask but is a mask for the selective deposition of a metal over an underlying layer of metal.

Regarding the use of a solder mask as opposed to the use of an isolation layer as provided by Mars, it is well known in the art that dispensing of a solder mask is:

- generally used where screening the mask is impractical because the affected component over which the solder mask is deposited has been already been partially populated with device elements
- in addition, solder mask dispensing provides a cost-effective alternative in high-mix, lower-volume environments, where the cost of developing screen fixtures for every assembly may be prohibitive

- solder mask depositions can flexibly adapt to specific requirements, such as masking a series of leads in a single dispense pass and/or masking multiple boards at the same time with dual or triple headed configurations, and
- in addition, commercially available solder mask deposition systems allow the manufacturer to easily optimize throughput, such as balancing the frequency of height sensing steps against the predicted amount of board warp and the overall specifications.

The above mentioned advantages and applications of a solder mask have been shown in order to more clearly distinguish between the use by Mars of a patterned layer of isolation, which is used to selectively deposit metal, and a solder mask as this solder mask is applied by the instant invention. From this listing it is respectfully suggested that it can be reasonably concluded that the two applications, a patterned layer of isolation material versus a solder mask, have no basis of commonality.

Forehand et al. provides an optimized routing scheme for an integrated circuit Printed Circuit Board (PCB). More specifically, Forehand et al. provides for a PCB having a

plurality of insulating layers and conductive layers, electrically conductive via plugs that extend through the PCB and flexibly interconnecting the via plugs and the conductive layers for the routing of voltages, increasing the layout capabilities of the IC in combination with the supporting PCB.

From the above provided summary of the Forehand invention, it is clear that many of the arguments that have been applied above with respect to the Yamai invention equally apply to the Forehand invention, more particularly where these comments relate to features of the instant invention that are not addressed or provided by the Forehand invention.

More specifically and as a partial repeat of the previously stated aspects provided by the instant invention, which are equally applicable in comparing the Forehand invention with the instant invention as not being provided by the Foreman invention, by applying fine pitch solder bumps directly to the I/O pads of a semiconductor device, the instant invention:

- enables that a redistribution interface is no longer needed, allowing for bonding the semiconductor device directly to a Ball Grid Array substrate using the flip-chip bonding approach

- provides for shortening the interconnection between a semiconductor device and the substrate on which the device is mounted, thus improving the electrical performance of the device
- provides for the elimination of conventional methods of re-distribution of device I/O interconnect, making packaging of the device more cost-effective and eliminating performance degradation
- provides for improved chip accessibility during testing of the device, thus eliminating the need for special test fixtures
- provides for improvements in performance and device reliability of BGA packages that are used for the mounting of semiconductor devices having small-pitch I/O interconnect bumps
- provides for a method of mounting small-pitch semiconductor devices in such a manner that flux removal and the dispensing of device encapsulants is improved
- provides a fine-pitch solder bump
- provides smaller solder bumps
- provides a fine-pitch solder bump of high reliability due to the increased height of the solder bump

- provides a cost-effective solder bump by using standard solder material and eliminating the need for expensive "low-α solder"
- provides a solder bump that allows easy cleaning of flux after the process of flip chip assembly and before the process of underfill and encapsulation, and
- a solder bump which allows easy application of underfill.

With respect to claim 13, the criticality of the solder balls being fine pitch is expressed in the specification in the following text, page 1 the second paragraph which highlights prior art needs and trends:

"Semiconductor device performance improvements are largely achieved by reducing device dimensions, a development that has at the same time resulted in considerable increases in device density and device complexity. These developments have resulted in placing increasing demands on the methods and techniques that are used to access the devices, also referred to as Input/Output (I/O) capabilities of the device."

which are addressed by the instant invention, as quoted from page 4 of the specification of the instant invention:

"The invention addresses concerns of creating a BGA type package whereby the pitch of the solder ball or solder bump of the device interconnect is in the range of 200 μm or less. The conventional, state-of-the-art solder process runs into limitations for such a fine interconnect pad pitch, the invention provides a method and a package for attaching devices having very small ball pitch to an interconnect medium such as a Printed Circuit Board.

With respect to claim 14, 15 and 16, the fine pitch solder bumps that are applied as part of the invention enable the arrangement of the solder mask in the manner specified, enabling the creation of a channel within the solder mask so that cleaning solution can flow there-through. The peripheral and center type pad design (claims 15, 16) of the electrical contacts are special design aspects of the instant invention that add design flexibility, providing for added package capabilities that may be advantageously applied for unique design requirements and implementations. For these reasons claims 14-16 are provided, providing unique and added packaging capabilities.

With respect to claims 19, 20 and 22, these claims specify further detail of creation of the package of the invention, detail that is required in order to accurately and completely make use of the unique aspects of the high-density package of the invention. The removal of the barrier layer is important in creating the solder bumps that form the small pitch solder bumps used by the package of the invention. This barrier material can be removed so that only the barrier layer that is covered by the pillar remains in place (claim 19) or so that an additional barrier layer remains in place surrounding the pillar (claim 20). In creating the package of the invention, it is further important to specify the step of removing flux from the surface of the BGA substrate, as specified in claim 22.

Regarding claims 21 and 24, these claims go to the very essence of the invention and to the solder bumps that support and are an integral part of the package of the invention. Without these claims 21 and 24, any solder bump could be used, without specifically providing detail of the pitch and the height of the solder bump on which the package of the invention is critically based.

While applicant acknowledges the teachings of Yamai and Forehand et al. and Mars as cited by the Examiner, and although applicant does not necessarily agree that the Examiner's arguments show sufficient and proper basis for suggestion or motivation to modify or combine Yamai with Forehand et al. and with Mars, applicant nonetheless also asserts that there is absent within the portions of Yamai and Forehand et al. and Mars or any combination thereof, as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's invention as taught and claimed within claim 13 and the dependent claims 14-24 of the instant invention.

In this regard, applicant claims that there is absent form the portions of Yamai and Forehand et al. and Mars, or any combination thereof, as cited by Examiner, a teaching of forming a semiconductor package as supported by claim 13 and the dependent claims to claim 8, which specify the details of how the semiconductor package is created, providing a process that is at significant variance with the process of Yamai and Forehand et al. and Mars since the latter processes do not address the creation of a semiconductor package.

To combine the teachings of Yamai and Forehand et al. and Mars is not obvious, since there is no suggestion or motivation

in the teachings of any of these patents of the present invention. The instant invention specifically provides a semiconductor package that combines fine pitch solder bump with BGA substrate technology. In the context of the instant invention, and not either supported by or inferred by or referred to by Yamai and Forehand et al. and Mars singly or in combination thereof, provides a semiconductor device package, comprising a semiconductor device having fine pitch, high reliability solder bumps provided over the active surface of the semiconductor device, a Ball Grid Array substrate, a solder mask provided over said second surface of said BGA substrate and further providing the interconnection of the device with the BGA substrate, making use of contact balls.

Applicant therefore asserts that there is absent within the portions of Yamai and Forehand et al. and Mars or any combination thereof, as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's invention as taught and claimed within claim 13 and the therewith specified supporting claims.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 13-16 and 18-24 under 35 U.S.C 103(a), be withdrawn.

2. Reconsideration of the rejection of claim 17 under 35 U.S.C 103(a) as being unpatentable over Yamai (JP 409045691) and Forehand et al. (U.S. Patent 5,847,936) and Mars (U.S. Patent 5,795,81) and further in combination with Pao et al. (U.S. Patent 5,931,371) is respectfully requested based on the following.

The relative merits of Yamai and Mars and Forehand with respect to the instant invention have been discussed in detail above and are enclosed at this time by reference.

Regarding claim 17, Pao et al. uses, Fig. 4, a standoff 28 that is created by applying reflow to solder paste 12 (Fig. 3). The standoff encapsulates a solder ball 18, whereby the reflow of solder paste 12 (Fig. 3) is carefully temperature controlled to assure that solder ball 18 does not simultaneously reflow with the solder paste 12. Solder paste 12 wets and overlies a bond pad 16. Solder ball 18 and adjacent solder paste 12 are shapes that have no commonality with the instant invention in the cross section that is shown after these two elements have

been formed, the solder ball 18 having a circular cross section while supporting paste 12 has a compound, platform shaped cross section.

The dummy solder bumps of the invention, as specified in claim 17, are, in accordance with the specification of claim 17, solder balls "being provided in addition to said fine pitch, high reliability solder bumps provided to said points of electrical contact in the active surface of said device". The dummy solder bumps of the instant invention are therefore solder bumps that by design are not actively used as interconnects.

From the cross section shown by Pao et al., Fig. 4, there cannot be derived a concept of solder bump pitch since solder ball 18 is the only solder ball in the configuration and therefore not adjacent to any other solder balls, therefore does not have a pitch. In addition, Pao et al. does not, contrary to Examiner's assertion, concern himself with fine pitch solder balls and makes no mention thereof in the specification.

It must in this respect be pointed out that, taking into account the above presented and referred to relative merits of Yami and Forehand and Mars with respect to the instant invention, that none of the applied or known references address

the invention as shown in the claim 17. The invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these various references cannot be made without reference to Applicant's own invention.

None of the applied references address the problem of creating a semiconductor package comprising fine pitch solder bumps directly connected to the I/O pads of a semiconductor device, without a redistribution interface, of shortening the interconnection between a semiconductor device and the substrate on which the device is mounted, thus improving the electrical performance of the device, of eliminate conventional methods of re-distribution of device I/O interconnect, of making packaging of the device more cost-effective and eliminating performance degradation, of improving chip accessibility during testing of the device, thus eliminating the need for special test fixtures, of improving package performance and package reliability of BGA packages, of various pad designs such as peripheral or central pad designs and of improving flux removal and the dispensing of device encapsulants.

Applicant has claimed his process in detail. The solder bumps and packages of Figs. 3-6 are both believed to be novel

and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable.

We believe that there is no such basis for the combination. We therefore request Examiner James M. Mitchell to reconsider his rejection in view of these arguments and the amendment to the claims.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claim 17 under 35 U.S.C 103(a), be withdrawn.

Other Considerations

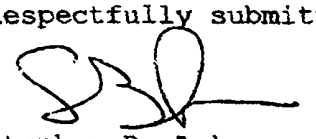
No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

A new method and package is provided for the mounting of semiconductor devices that have been provided with small-pitch Input/Output interconnect bumps. Fine pitch solder bumps, consisting of pillar metal and a solder bump, are applied directly to the I/O pads of the semiconductor device, the device is then flip-chip bonded to a substrate. Dummy bumps may be provided for cases where the I/O pads of the device are arranged such that additional mechanical support for the device is required.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



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points of electrical contact provided over said second surface of said BGA substrate by a process of solder reflow.

12. The method of claim 1, said height of columns of pillar metal being between about 10 and 100 μm and more preferably about 50 μm.

13. A semiconductor device package, comprising:

a semiconductor device, said device having been provided with points of electrical contact in an active surface thereof, said points of electrical contact having been provided with fine pitch, high reliability solder bumps, said solder bumps extending from said active surface of said semiconductor device over a height of columns of pillar metal, said columns of pillar metal being in contact with said points of electrical contact provided in the active surface of said semiconductor device;

a Ball Grid Array substrate, said BGA substrate having been provided with points of electrical contact over a first and a second surface thereof, said points of electrical contact provided over the second surface of said BGA substrate being connected to interconnect lines provided over the second surface of said BGA substrate;

a solder mask provided over said second surface of said BGA substrate;

said device being positioned over the second surface of said BGA substrate, said fine pitch, high reliability solder bumps facing said second surface of said BGA substrate, providing contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate;

electrical contact having been established between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate by a process of solder reflow;

said semiconductor device being encapsulated in a molding compound, said molding compound surrounding said device on all sides including said active surface of said device;

contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate; and

electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

14. The semiconductor device package of claim 13, said solder mask provided over said second surface of said BGA substrate

being removed from said points of electrical contact provided over the second surface of said BGA substrate by a measurable amount, creating a channel through which cleaning solution can readily flow.

15. The semiconductor device package of claim 13, said points of electrical contact provided in an active surface of said device comprising a peripheral pad design.

16. The semiconductor device package of claim 13, said points of electrical contact provided in an active surface of said device comprising a center type pad design.

17. The semiconductor device package of claim 16, dummy solder bumps having been provided over the active surface of said device, providing mechanical support for said device, said dummy solder bumps being provided in addition to said fine pitch, high reliability solder bumps provided to said points of electrical contact in the active surface of said device.

18. The semiconductor device package of claim 13, said fine pitch, high reliability solder bumps provided to said device comprising:

a layer of dielectric deposited over the active surface of said device, openings having been created in said layer of dielectric in a pattern overlying said points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

a layer of passivation deposited over the surface of said layer of dielectric, including the exposed surface of said points of electrical contact in an active surface of said device, openings having been created in said layer of passivation in a pattern overlying said points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

a layer of metal barrier deposited over the surface of said layer of passivation, including the exposed surface of said points of electrical contact in an active surface of said device;

pillar metal and solder bumps overlying said layer of barrier metal in a pattern overlying said points of electrical contact in an active surface of said device, said pillar metal and solder bumps being separated by a layer of under bump metal; and

said layer of barrier metal having been etched.

19. The semiconductor device package of claim 18, said etching said layer of barrier metal having removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal.

20. The semiconductor device package of claim 18, said etching said layer of barrier metal having removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal while further leaving in place said barrier layer extending from said pillar metal by a measurable amount.

21. The semiconductor device package of claim 13, said points of electrical contact in an active surface of said device having a pitch of about 200 μm or less.

22. The semiconductor device package of claim 13, flux removal from a gap between said second surface of said BGA substrate and said active surface of said semiconductor device having been performed after completion of flip chip assembly and solder reflow.

23. The semiconductor device package of claim 13, said encapsulation of said semiconductor device in a molding compound being replaced with an underfill for said device.

24. The semiconductor device package of claim 13, said height of columns of pillar metal being between about 10 and 100 μm and more preferably about 50 μm.